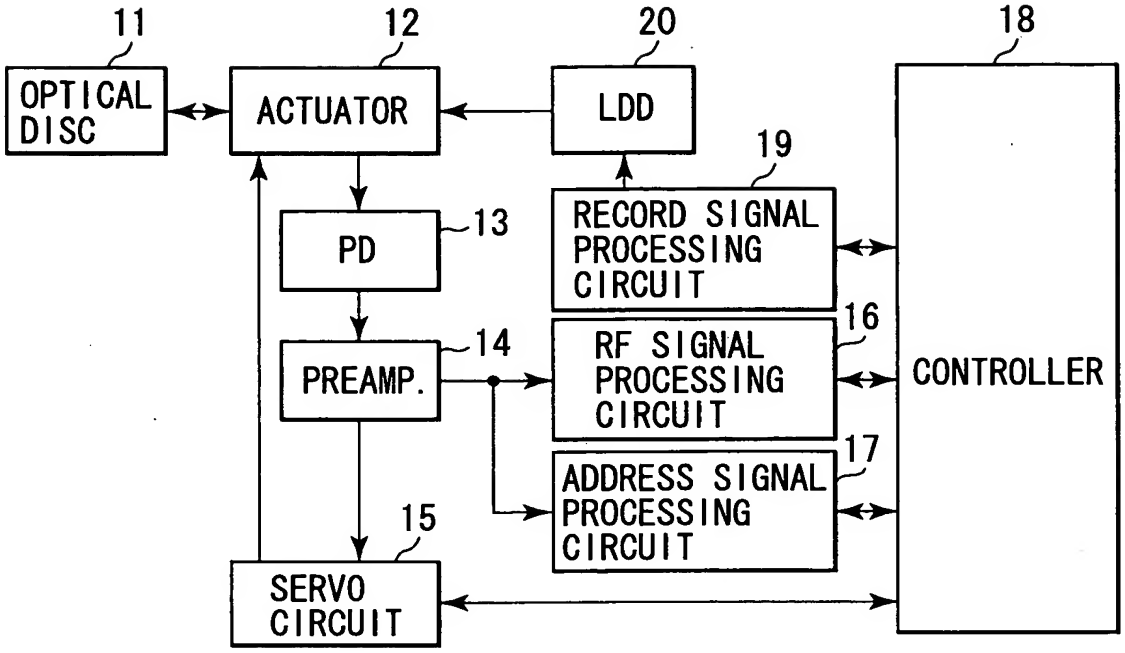

11
12
20
18
OPTICAL DISC
ACTUATOR
LDD
19
RECORD SIGNAL PROCESSING CIRCUIT
PD
13
16
PREAMP.
14
RF SIGNAL PROCESSING CIRCUIT
CONTROLLER
17
ADDRESS SIGNAL PROCESSING CIRCUIT
15
SERVO CIRCUIT

FIG. 1

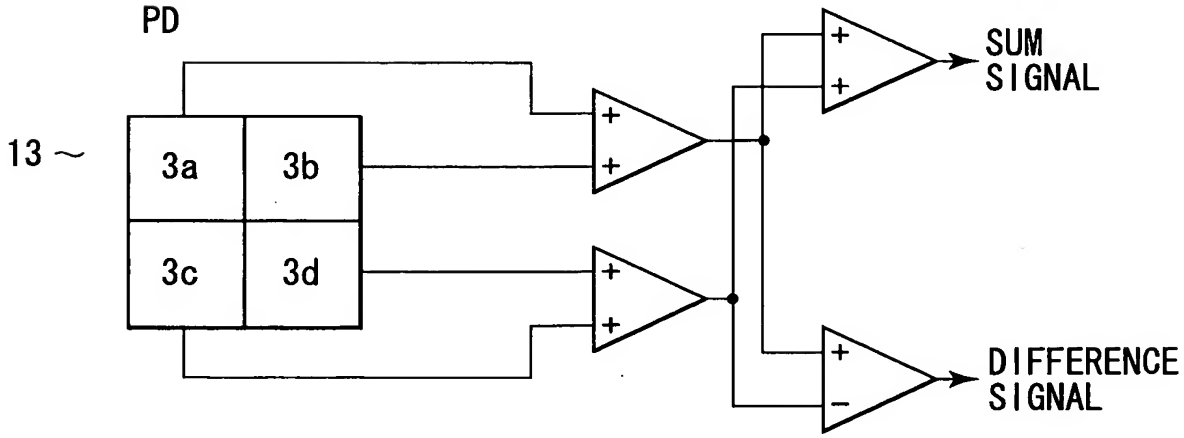

PD
13
3a
3b
3c
3d
SUM SIGNAL
DIFFERENCE SIGNAL

FIG. 2

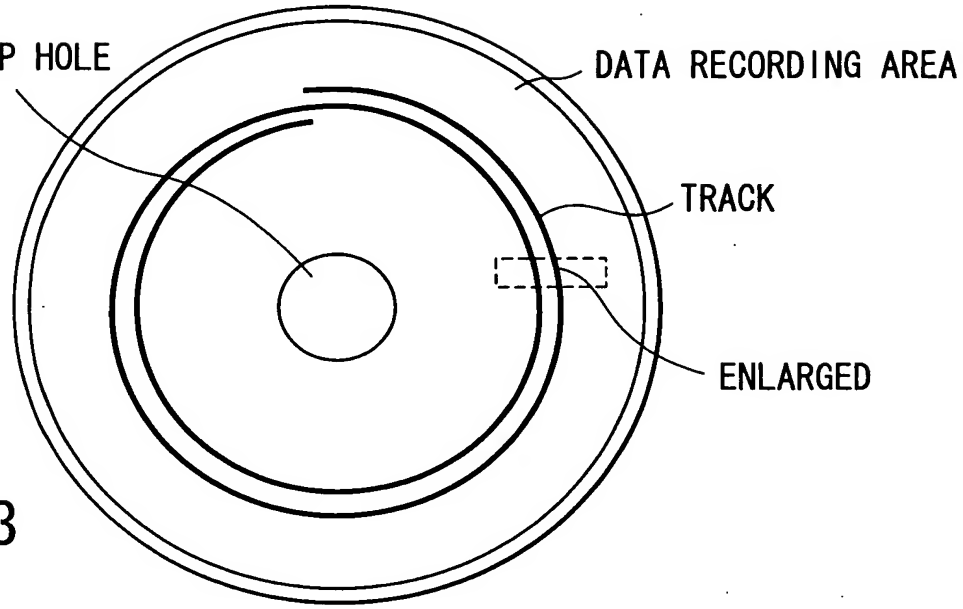


FIG. 3

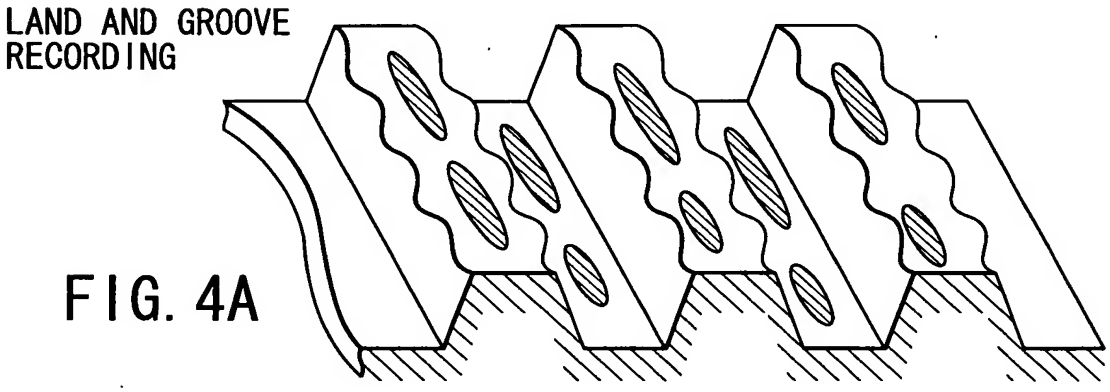


FIG. 4A

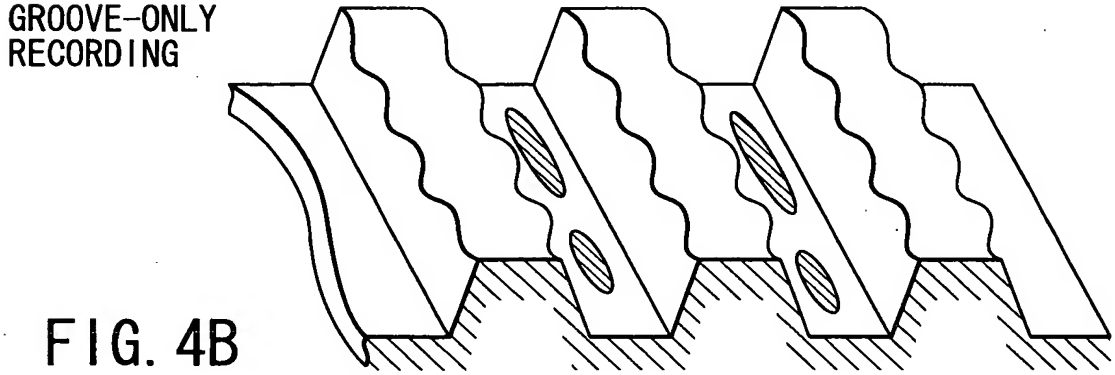


FIG. 4B

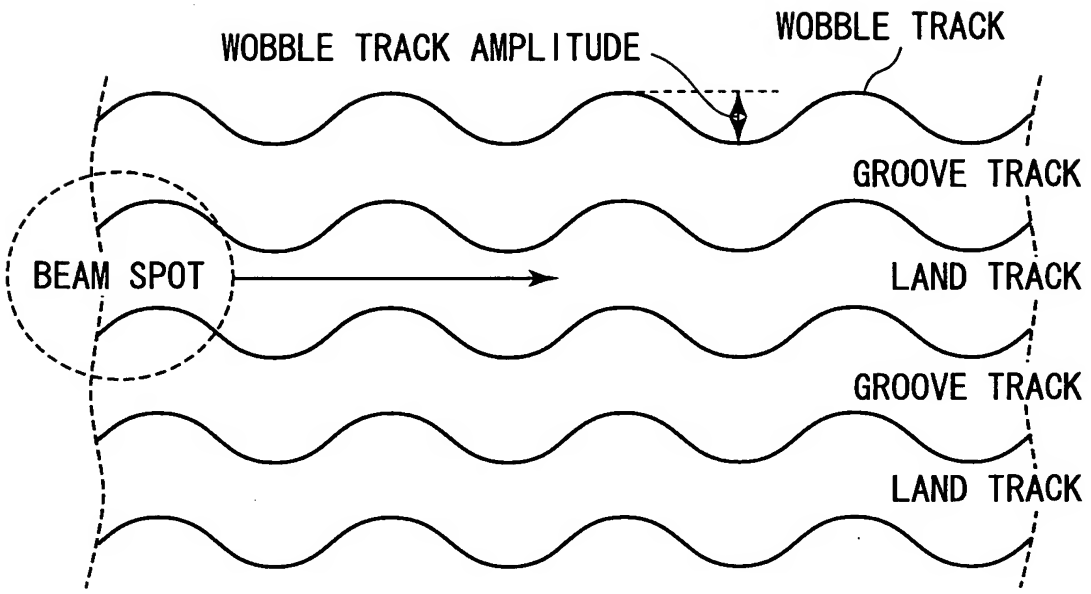


FIG. 5

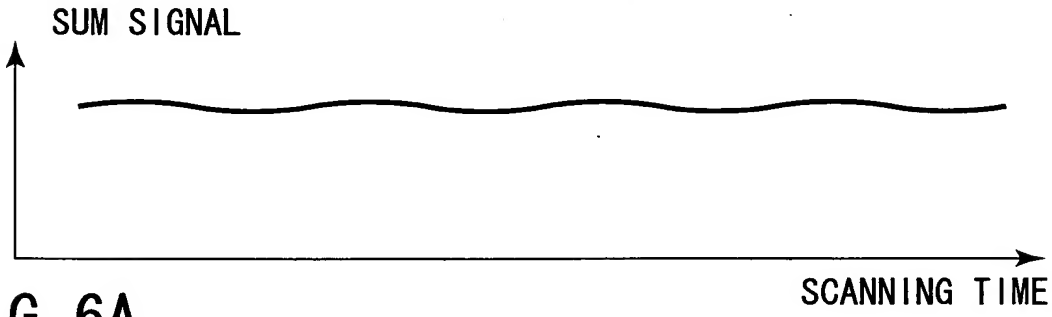


FIG. 6A

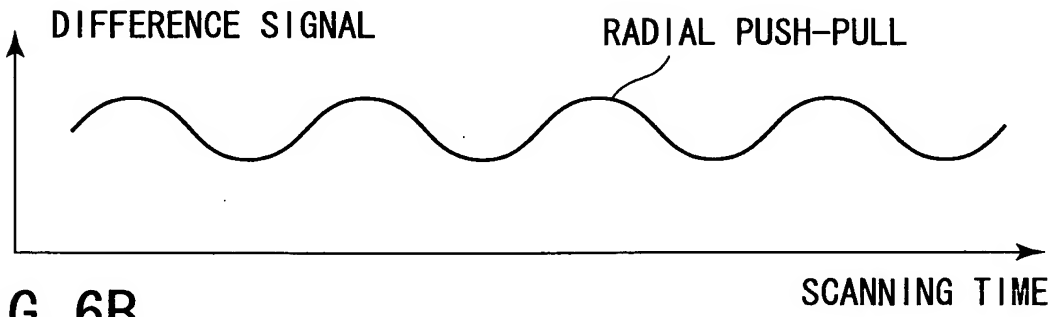


FIG. 6B

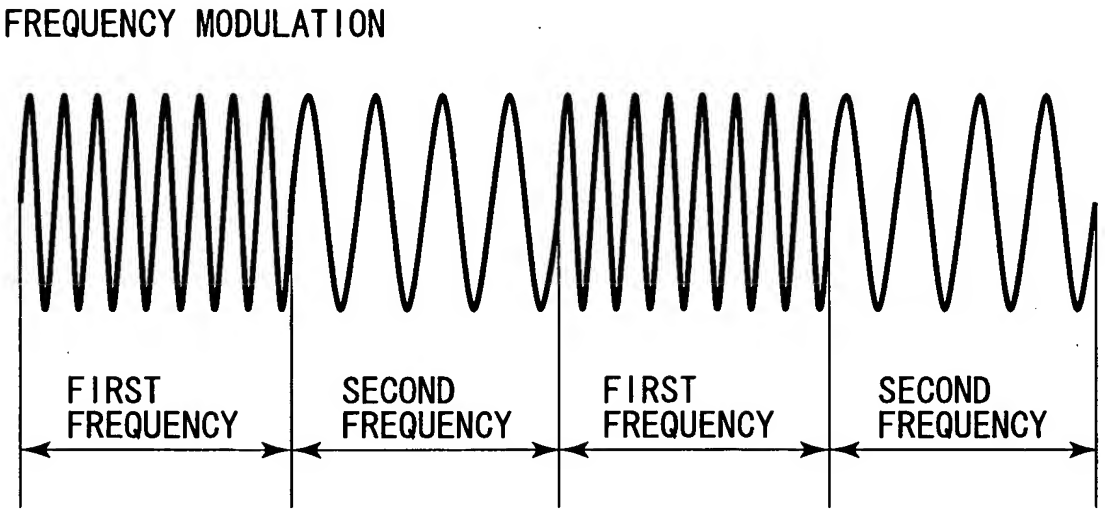

FREQUENCY MODULATION
FIRST FREQUENCY
SECOND FREQUENCY
FIRST FREQUENCY
SECOND FREQUENCY

FIG. 7

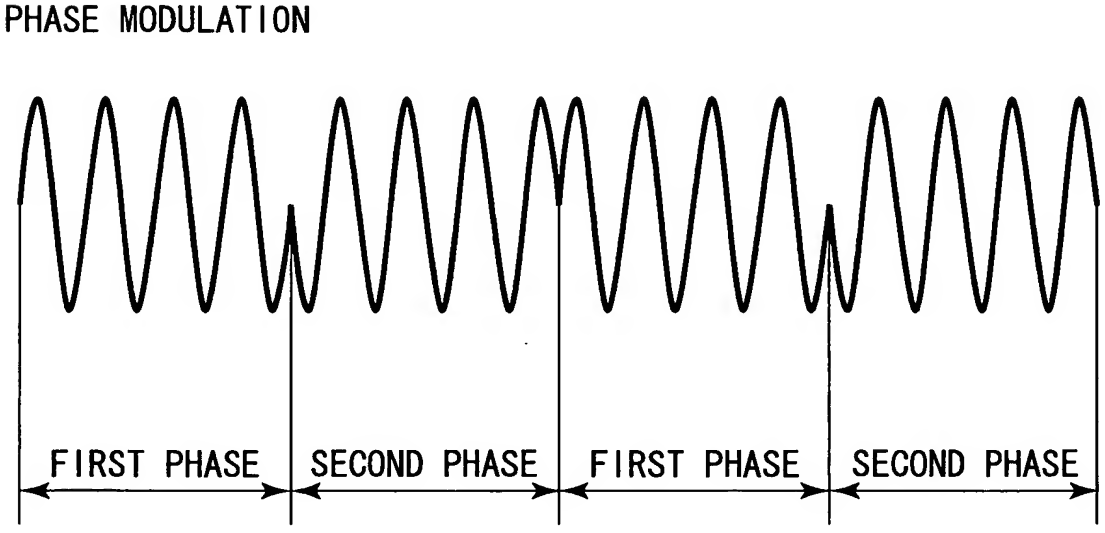

PHASE MODULATION
FIRST PHASE
SECOND PHASE
FIRST PHASE
SECOND PHASE

FIG. 8

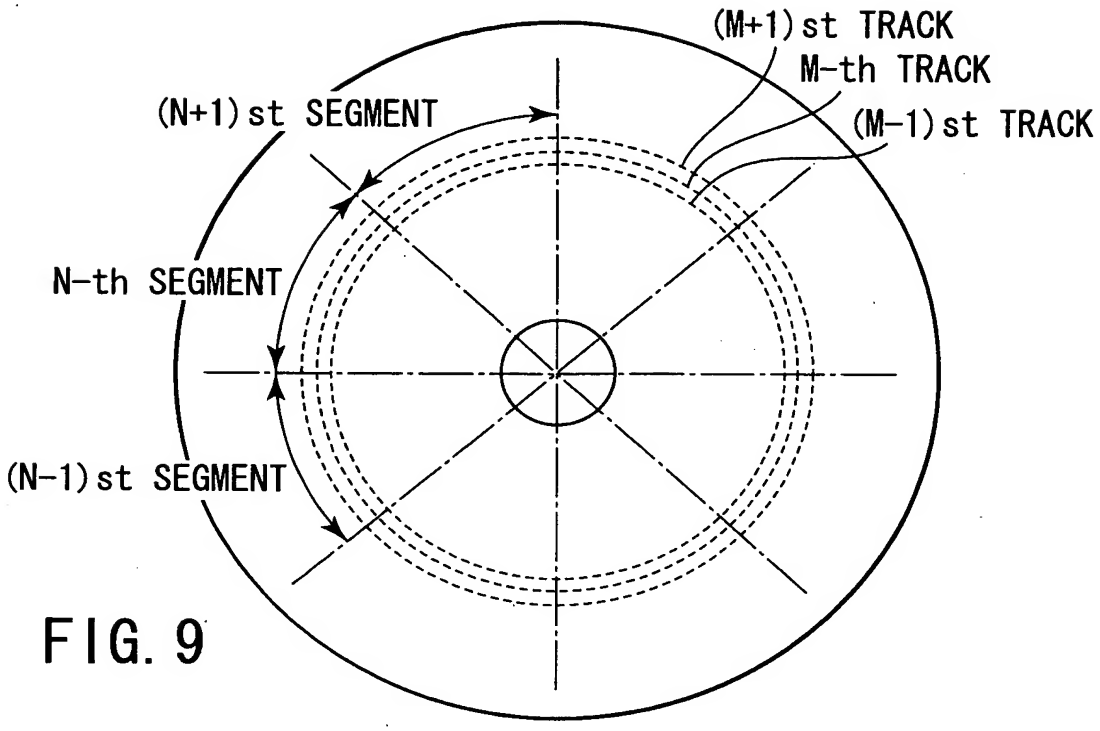

(M+1)st TRACK
M-th TRACK
(M-1)st TRACK
(N+1)st SEGMENT
N-th SEGMENT
(N-1)st SEGMENT

FIG. 9

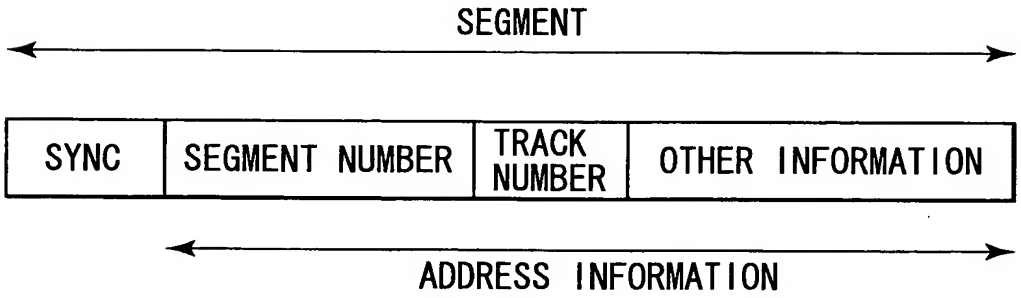

SEGMENT
SYNC
SEGMENT NUMBER
TRACK NUMBER
OTHER INFORMATION
ADDRESS INFORMATION

FIG. 10

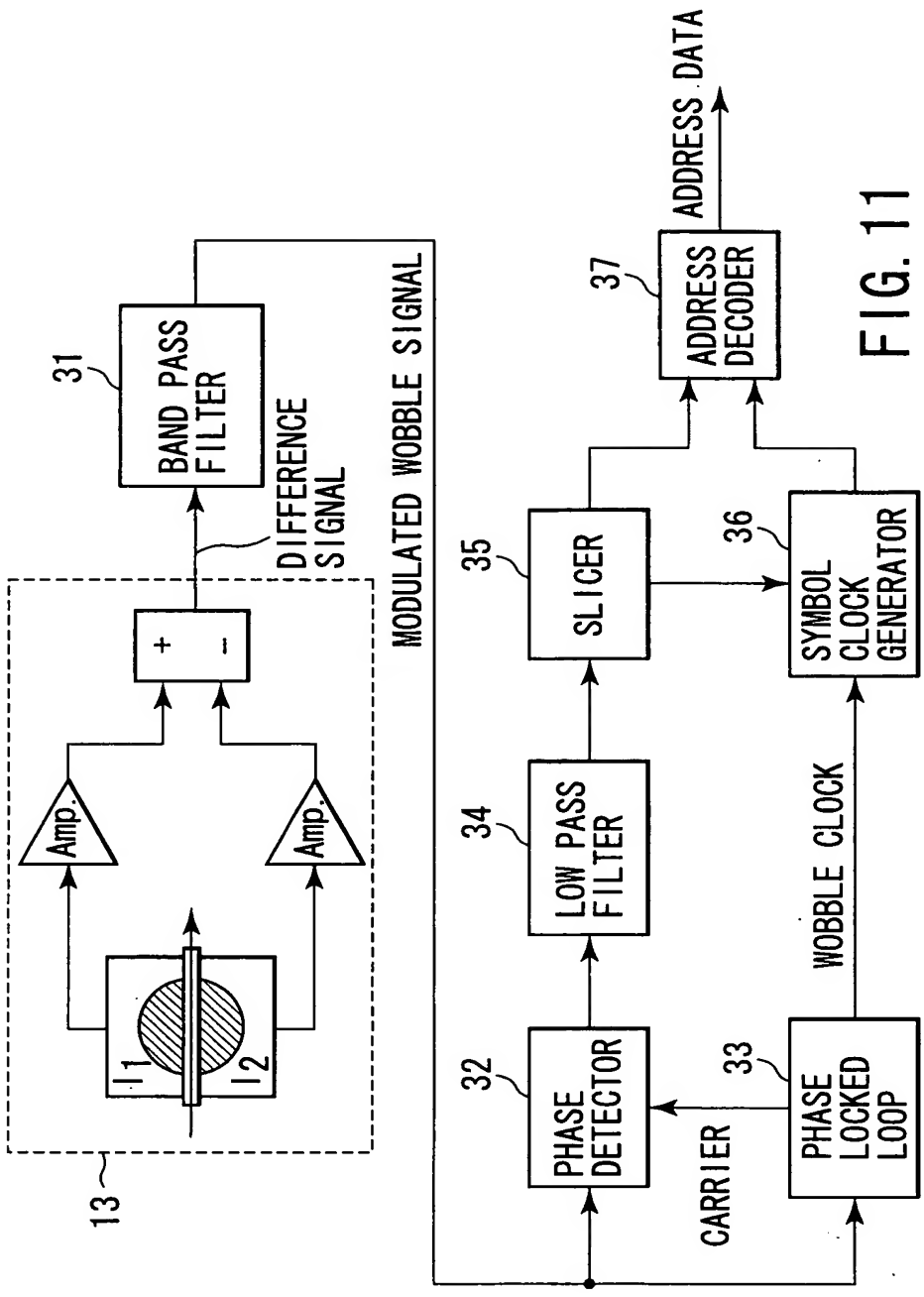

13
I1
I2
Amp.
Amp.
+
-
DIFFERENCE SIGNAL
31
BAND PASS FILTER
MODULATED WOBBLE SIGNAL
32
PHASE DETECTOR
34
LOW PASS FILTER
35
SLICER
37
ADDRESS DECODER
ADDRESS DATA
CARRIER
33
PHASE LOCKED LOOP
WOBBLE CLOCK
36
SYMBOL CLOCK GENERATOR

FIG. 11

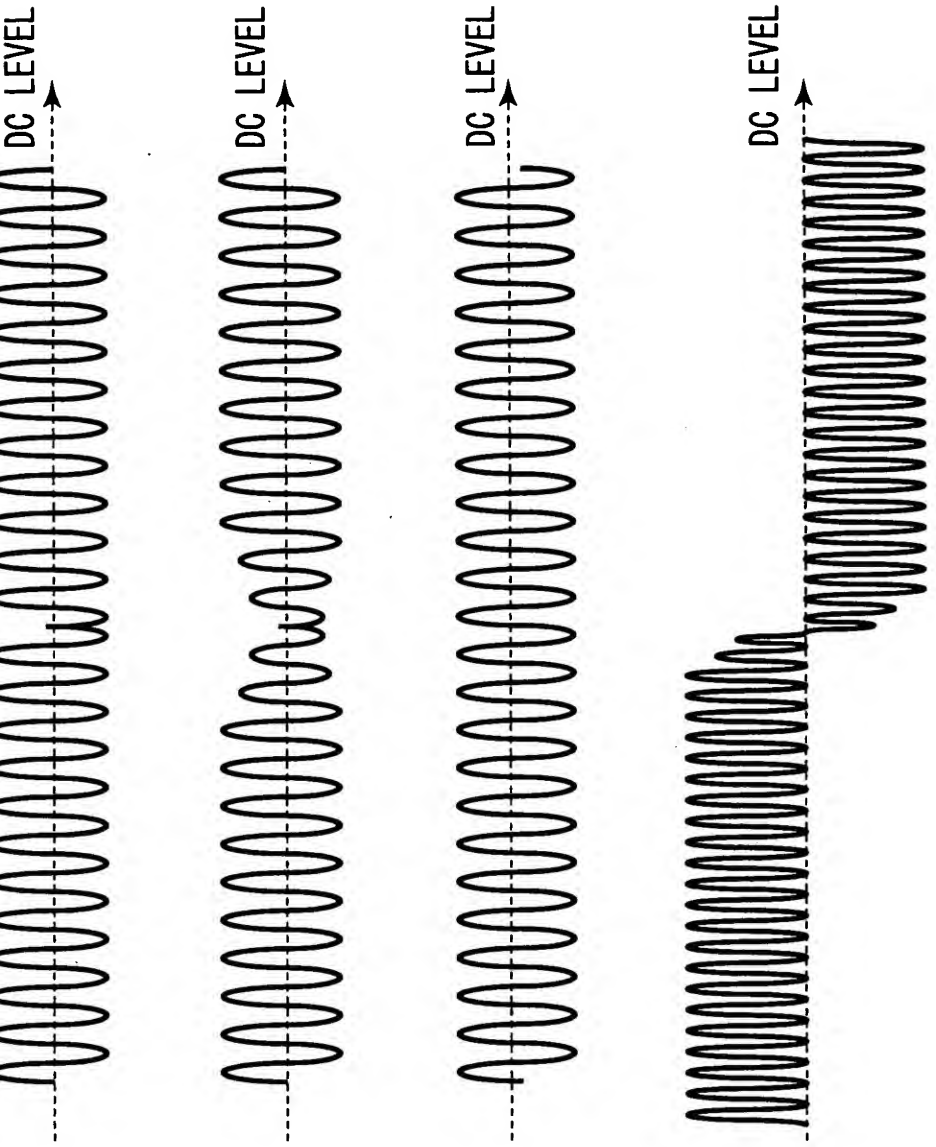


FIG. 12A

FIG. 12B

FIG. 12C

FIG. 12D

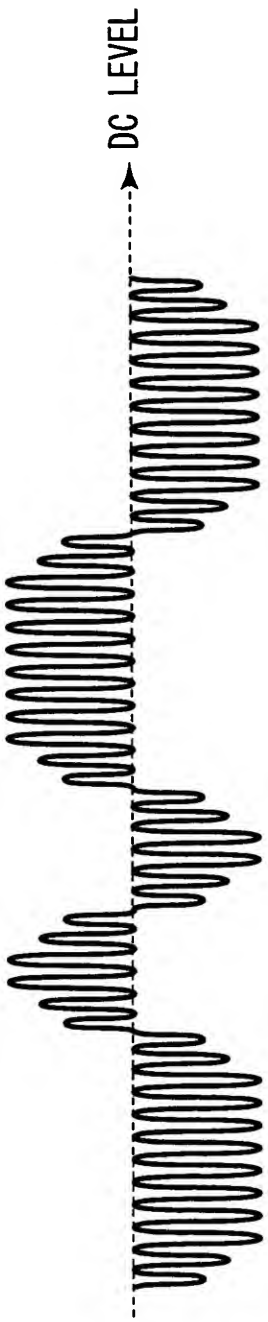


FIG. 13A

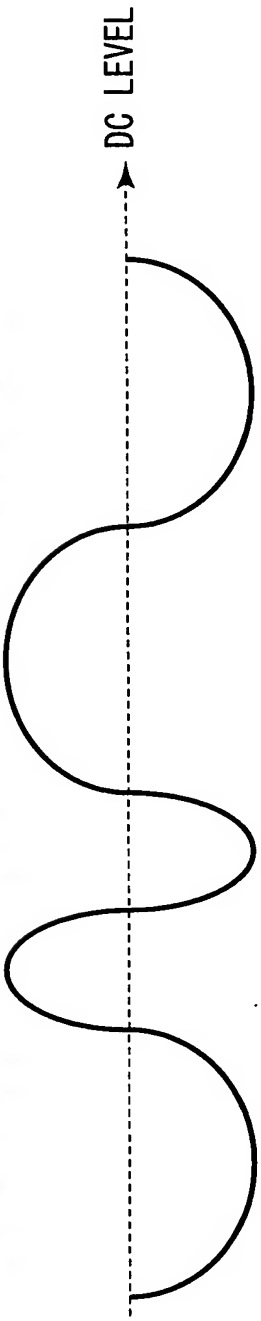


FIG. 13B

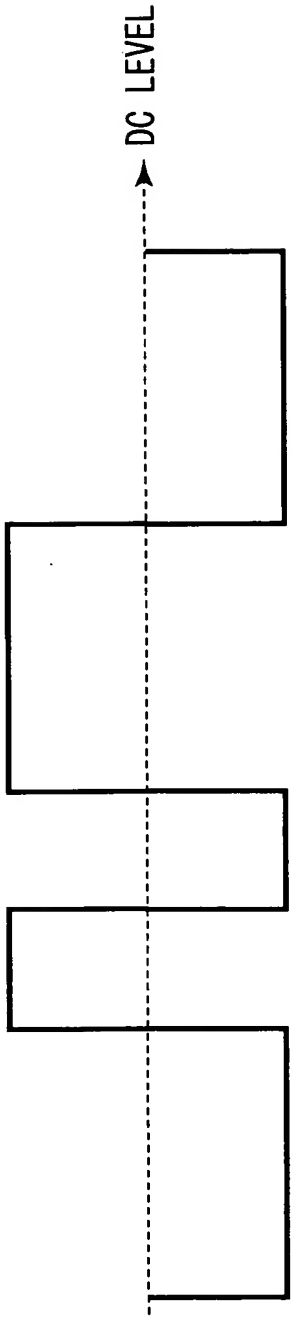


FIG. 13C

FIG. 13D

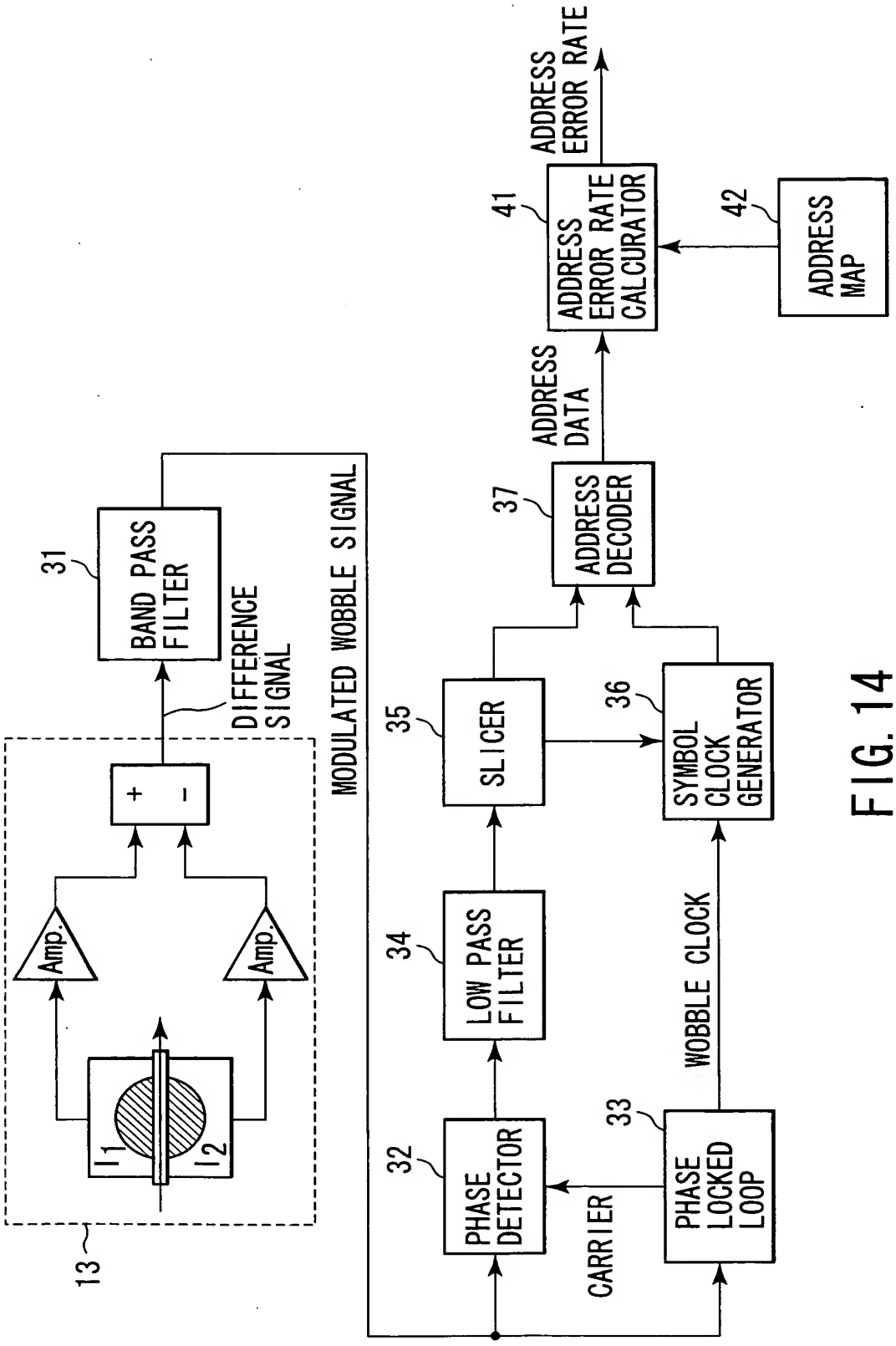

ADDRESS ERROR RATE
41
ADDRESS ERROR RATE CALCURATOR
42
ADDRESS MAP
ADDRESS DATA
37
ADDRESS DECODER
31
BAND PASS FILTER
DIFFERENCE SIGNAL
MODULATED WOBBLE SIGNAL
35
SLICER
36
SYMBOL CLOCK GENERATOR
34
LOW PASS FILTER
WOBBLE CLOCK
32
PHASE DETECTOR
33
PHASE LOCKED LOOP
CARRIER
Amp.
Amp.
+
-
I1
I2
13

FIG. 14

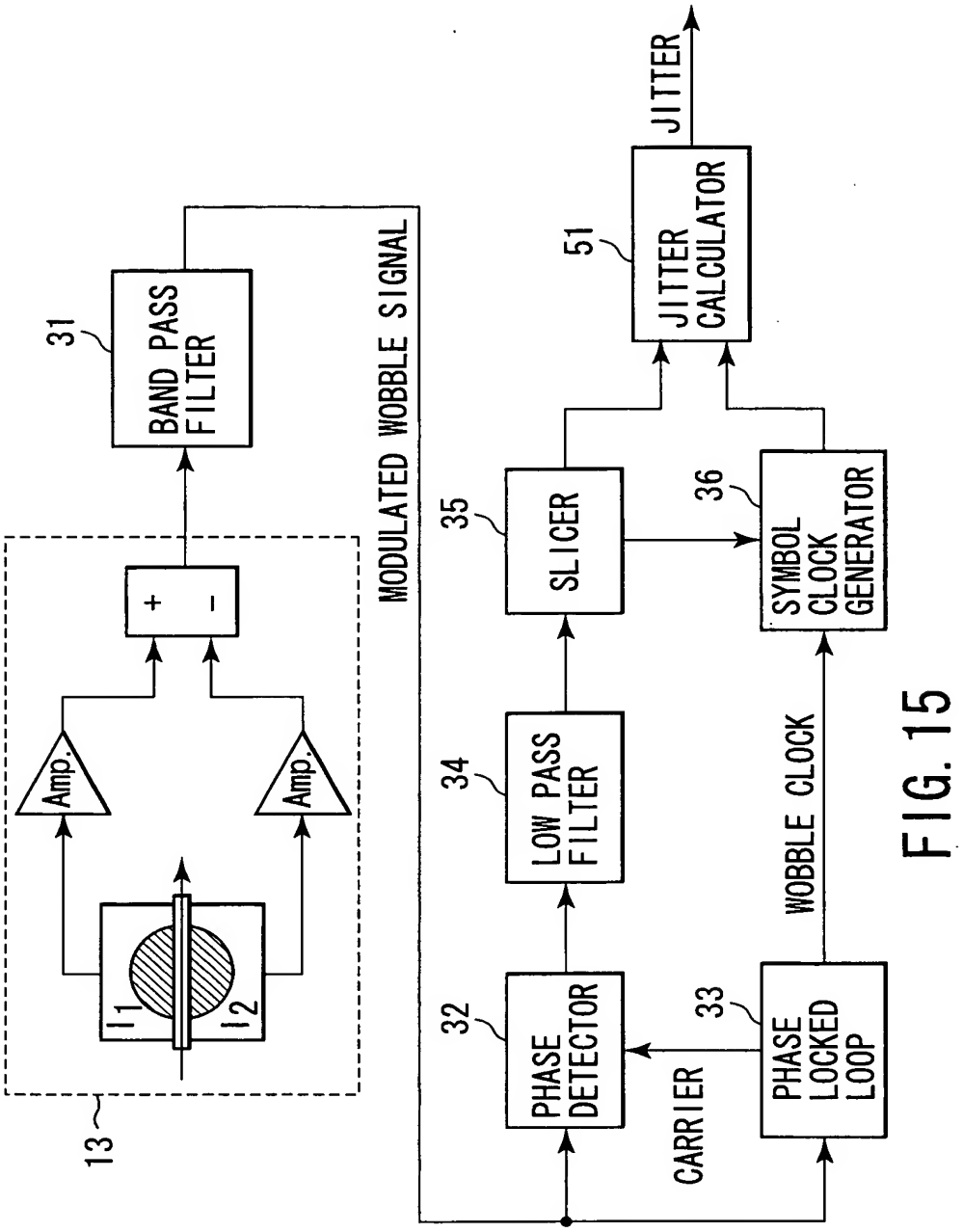

13
I1
I2
Amp.
Amp.
+
-
31
BAND PASS FILTER
MODULATED WOBBLE SIGNAL
32
PHASE DETECTOR
34
LOW PASS FILTER
35
SLICER
51
JITTER CALCULATOR
JITTER
CARRIER
33
PHASE LOCKED LOOP
WOBBLE CLOCK
36
SYMBOL CLOCK GENERATOR

FIG. 15

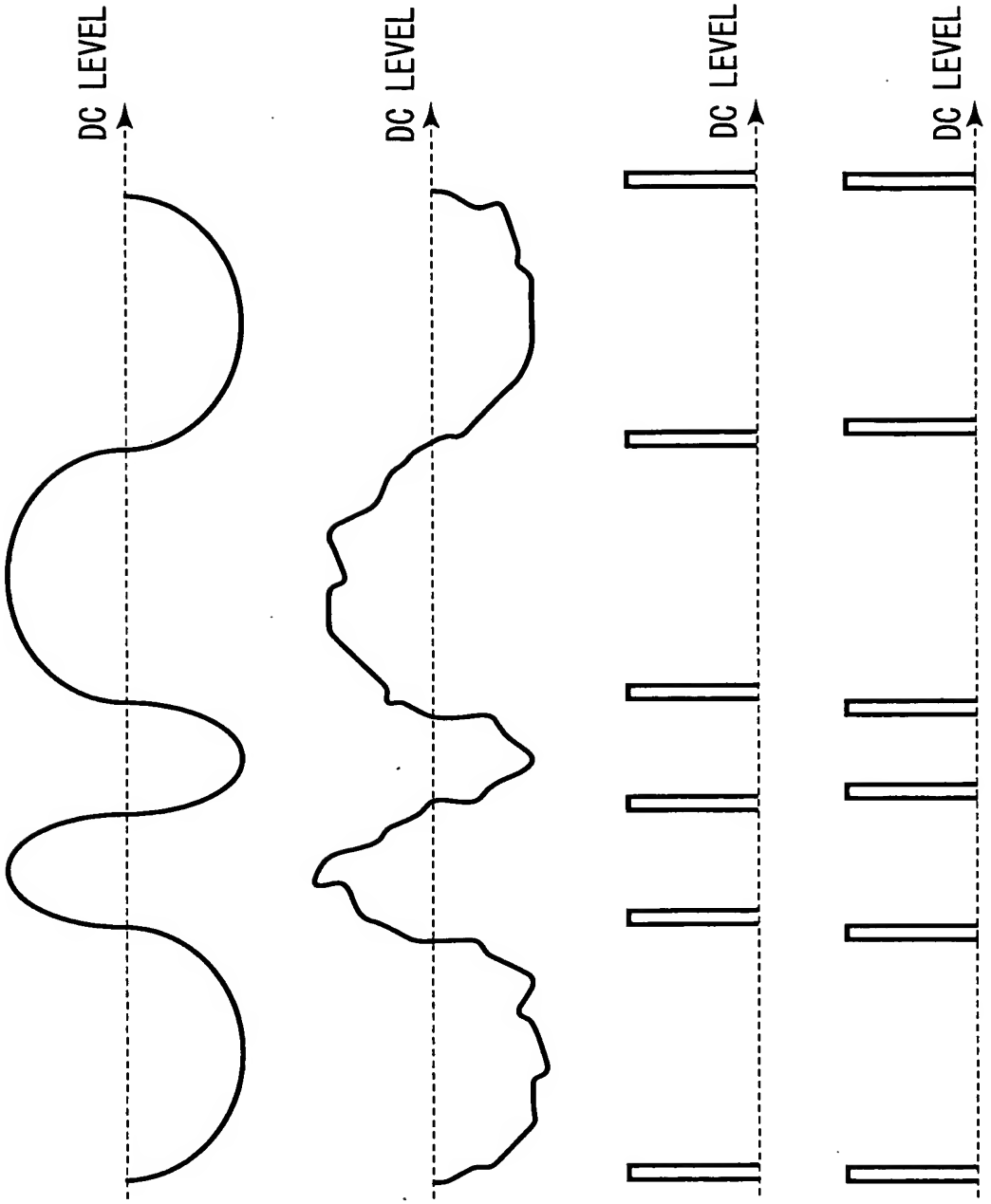


FIG. 16A

FIG. 16B

FIG. 16C

FIG. 16D

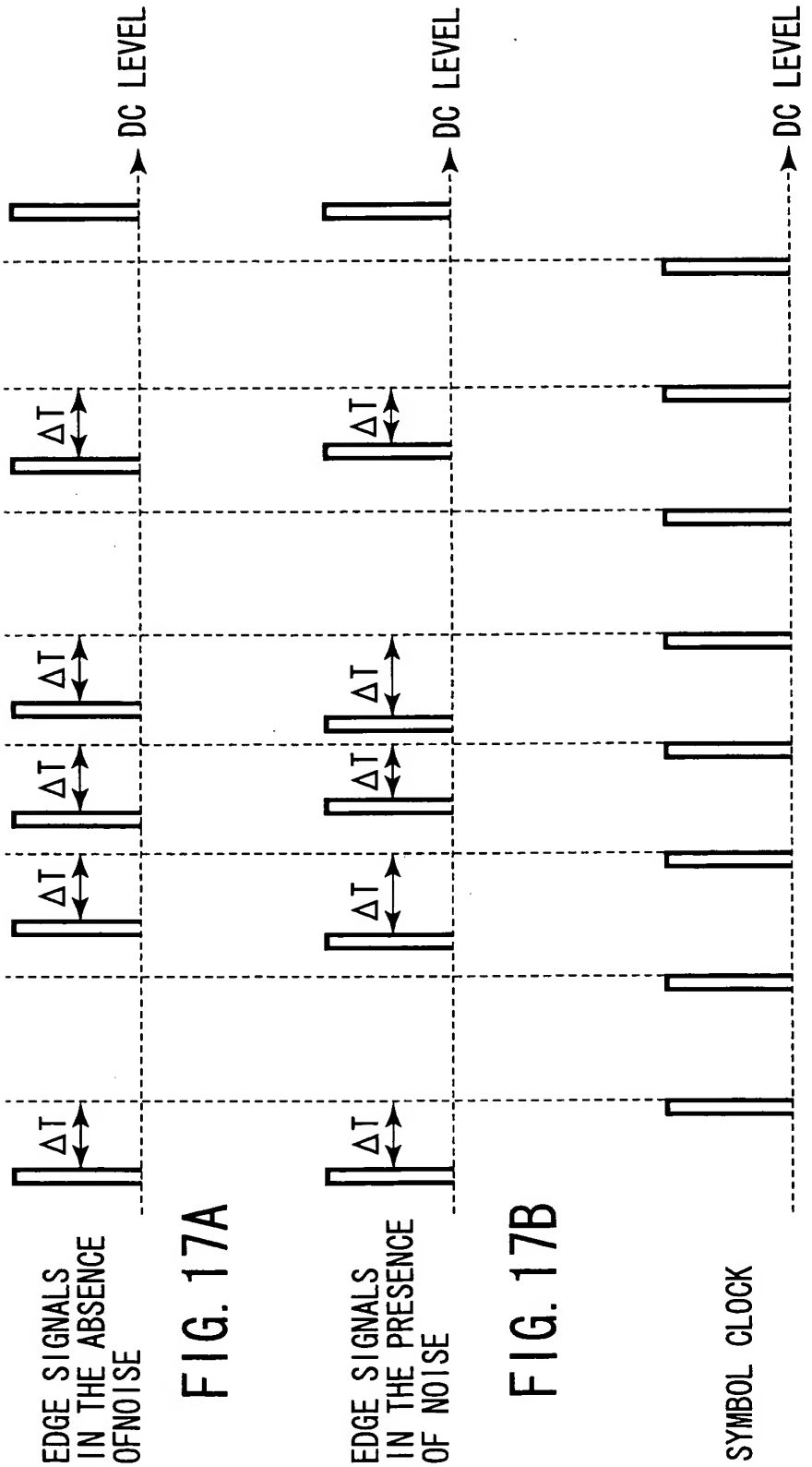


FIG. 17A

FIG. 17B

FIG. 17C

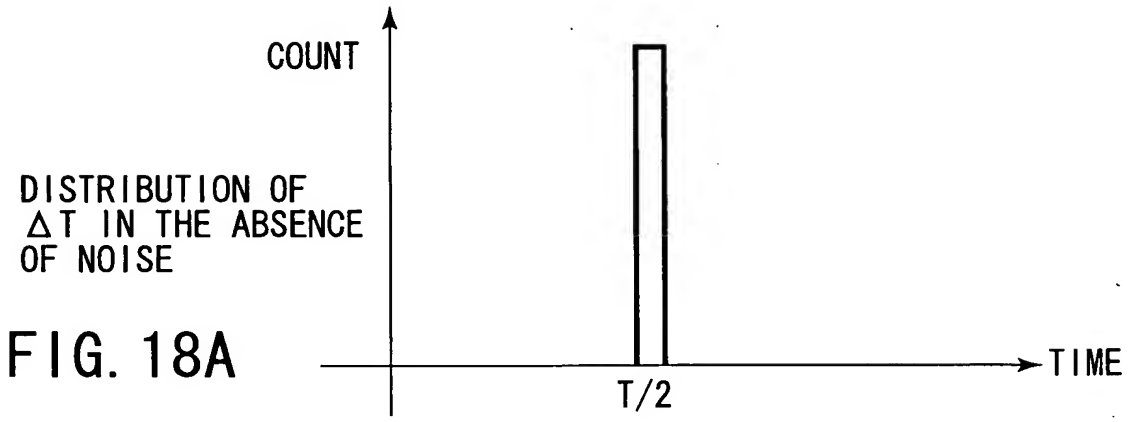


FIG. 18A

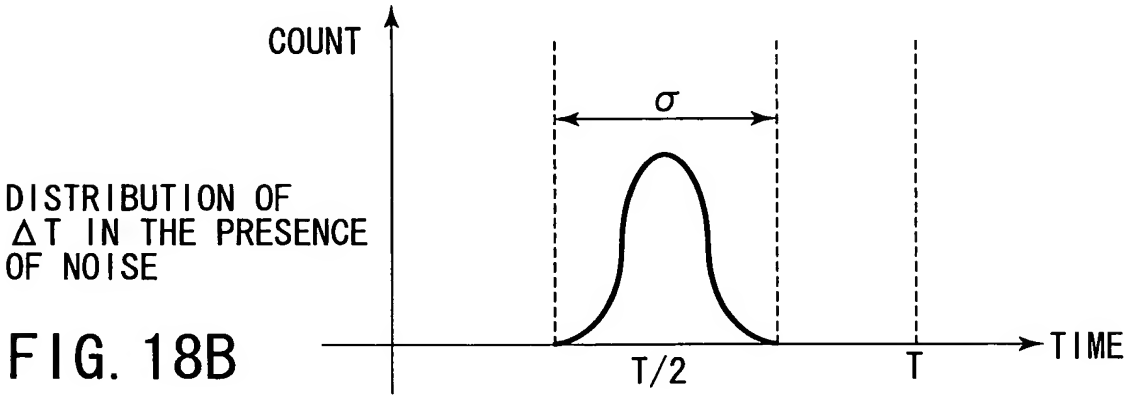


FIG. 18B

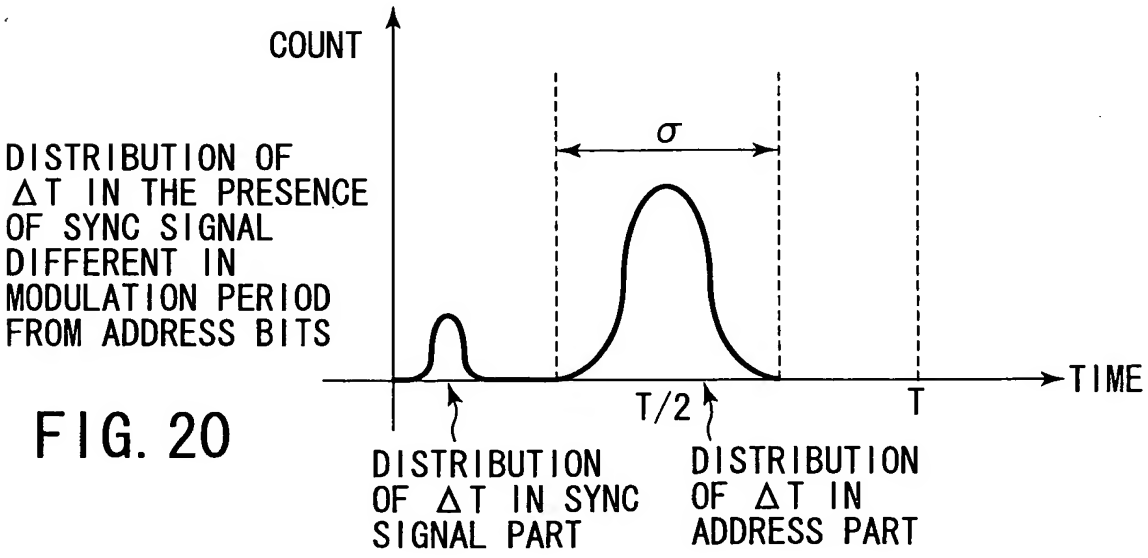


FIG. 20

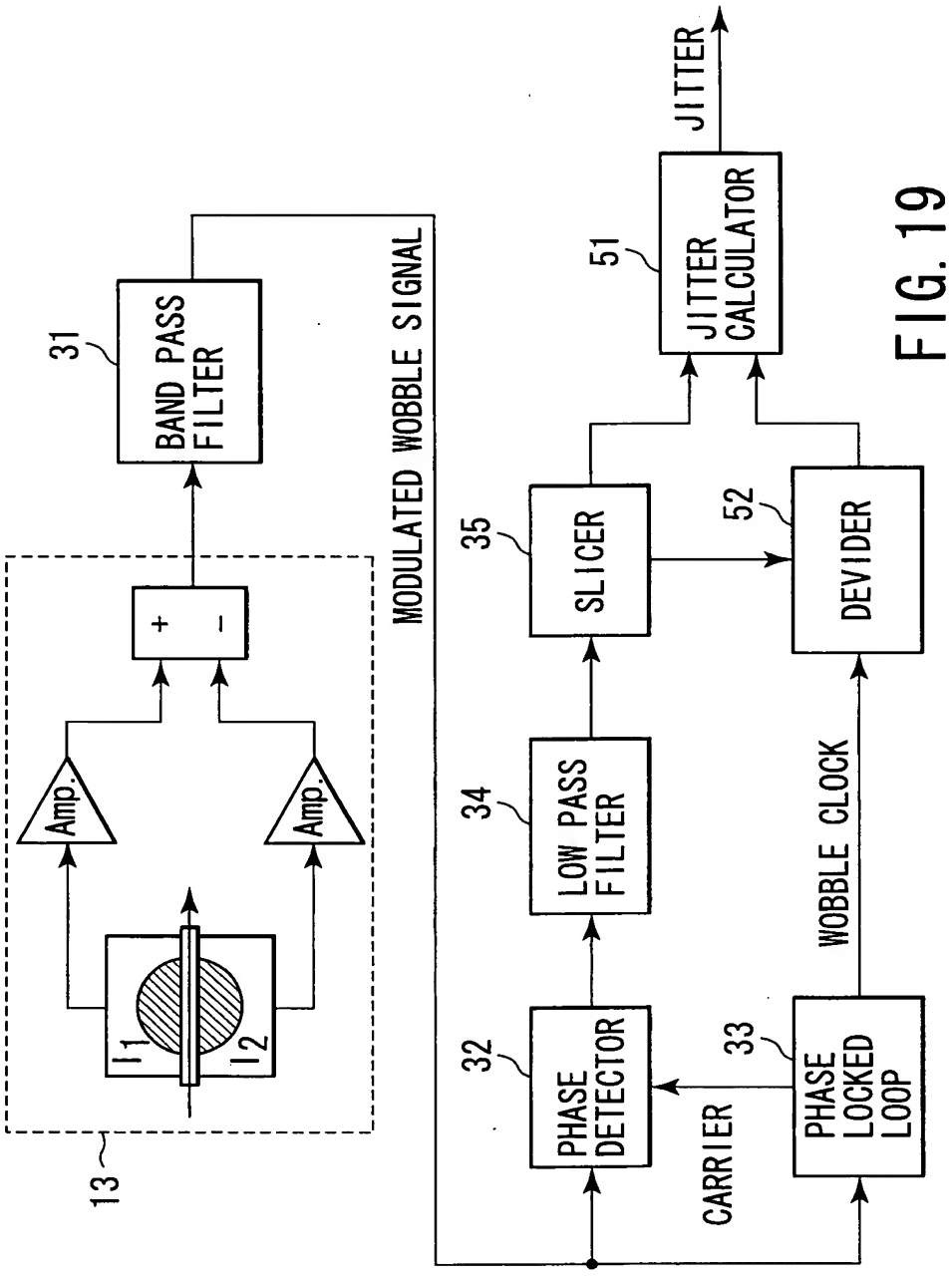

13
Amp.
Amp.
I1
I2
+
-
31
BAND PASS FILTER
MODULATED WOBBLE SIGNAL
35
SLICER
34
LOW PASS FILTER
32
PHASE DETECTOR
CARRIER
33
PHASE LOCKED LOOP
WOBBLE CLOCK
52
DEVIDER
51
JITTER CALCULATOR
JITTER

FIG. 19

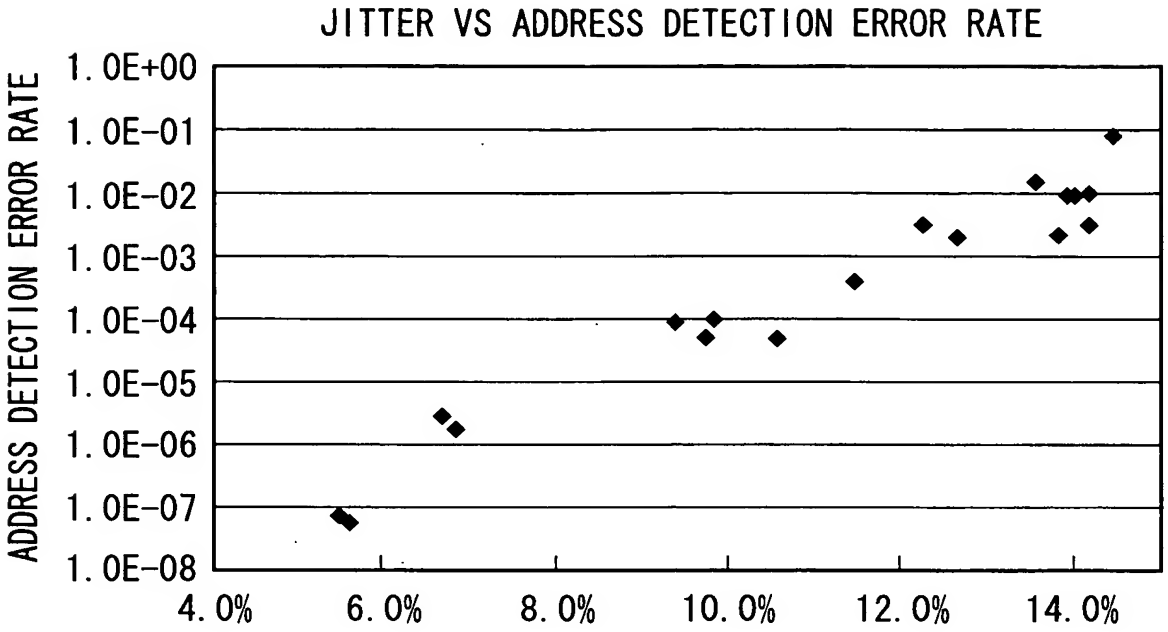

JITTER VS ADDRESS DETECTION ERROR RATE
ADDRESS DETECTION ERROR RATE
1.0E+00
1.0E-01
1.0E-02
1.0E-03
1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
4.0%
6.0%
8.0%
10.0%
12.0%
14.0%
JITTER (σ/T)

FIG. 21

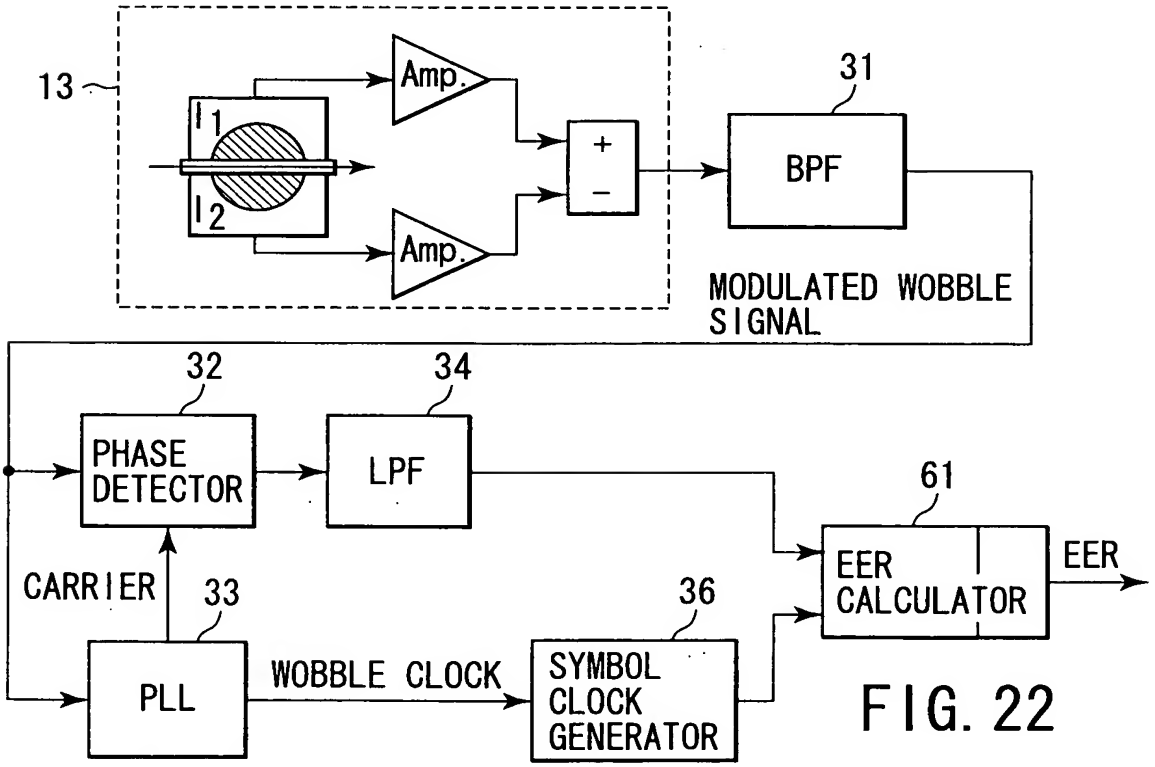

13
I1
I2
Amp.
Amp.
+
−
31
BPF
MODULATED WOBBLE SIGNAL
32
PHASE DETECTOR
34
LPF
61
EER CALCULATOR
EER
CARRIER
33
PLL
WOBBLE CLOCK
36
SYMBOL CLOCK GENERATOR

FIG. 22

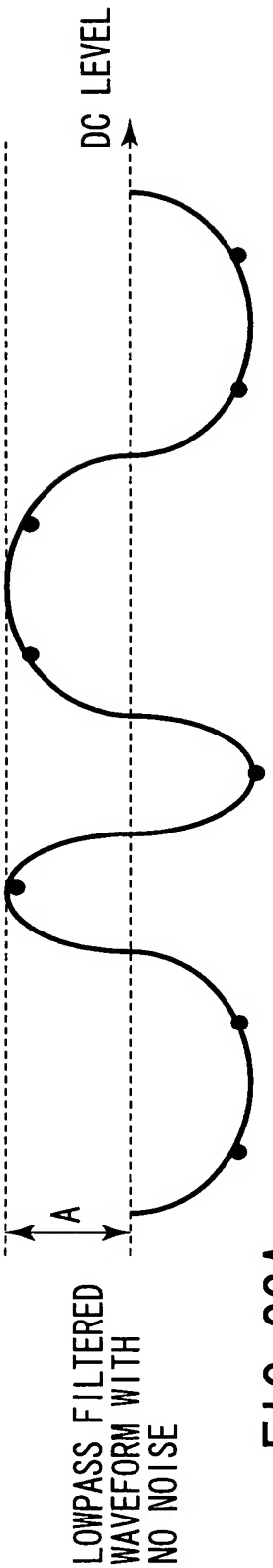


FIG. 23A

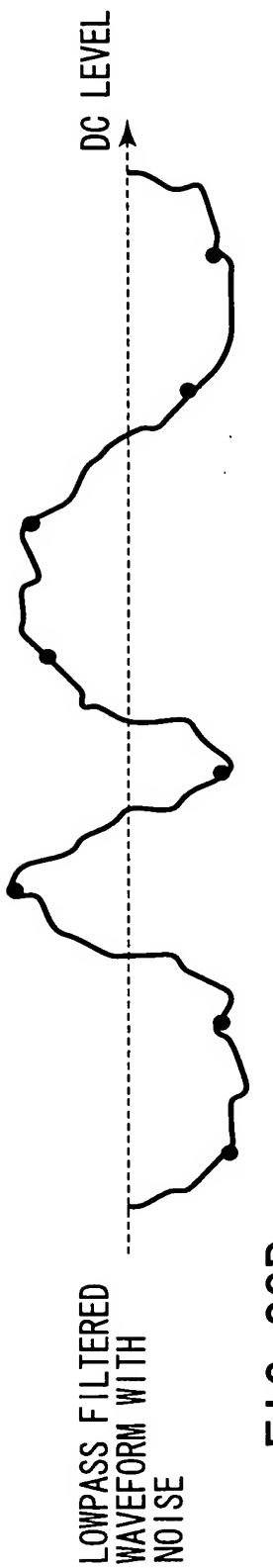


FIG. 23B

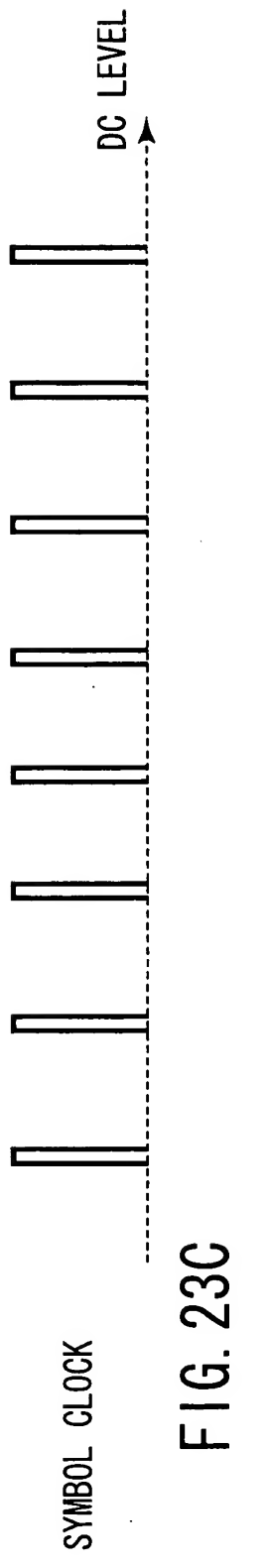
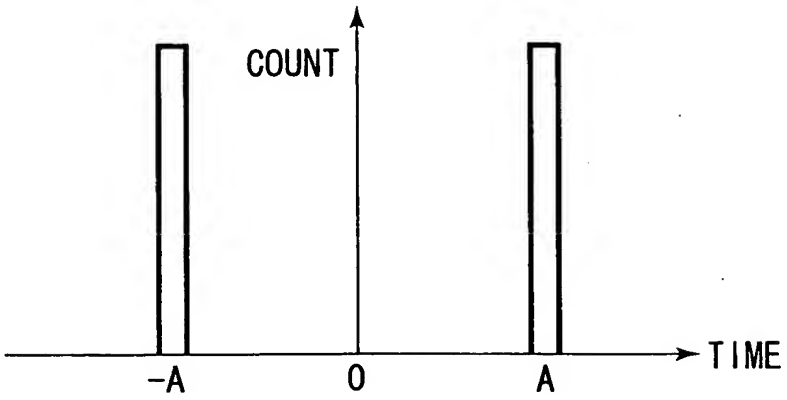


FIG. 23C

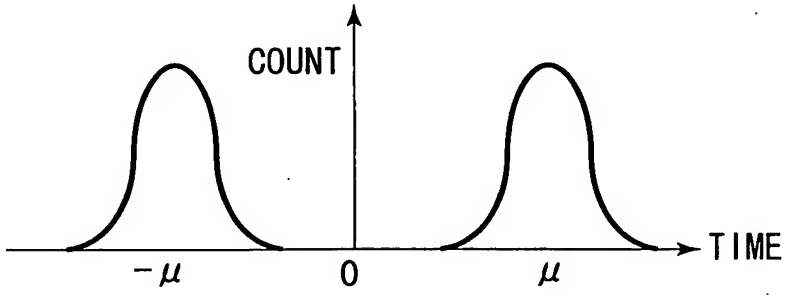
DISTIBUTION OF AMPLITUDES IN THE ABSENCE OF NOISE

FIG. 24A



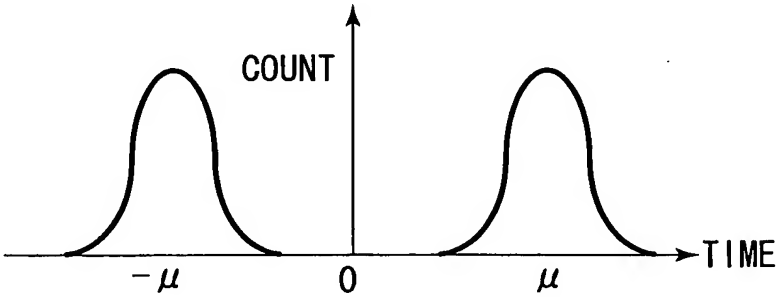
DISTIBUTION OF AMPLITUDES IN THE PRESENCE OF NOISE

FIG. 24B



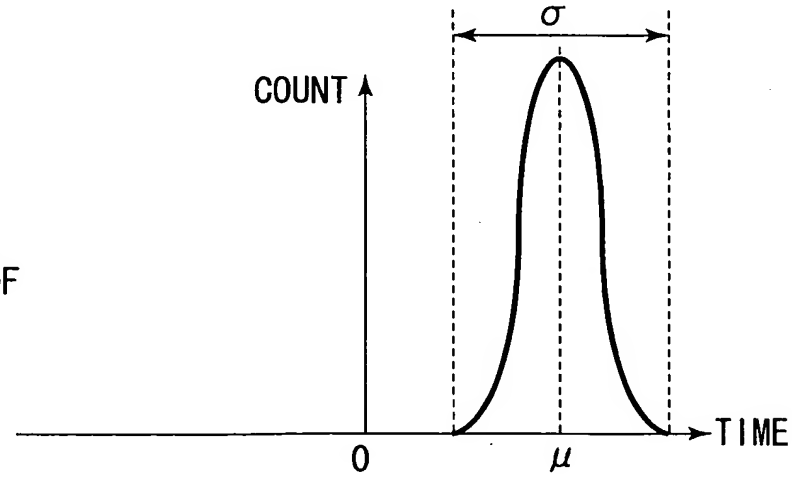
DISTIBUTION OF AMPLITUDES IN THE PRESENCE OF NOISE

FIG. 25A



DISTIBUTION OF ABSOLUTE-VALUE AMPLITUDES IN THE PRESENCE OF NOISE

FIG. 25B



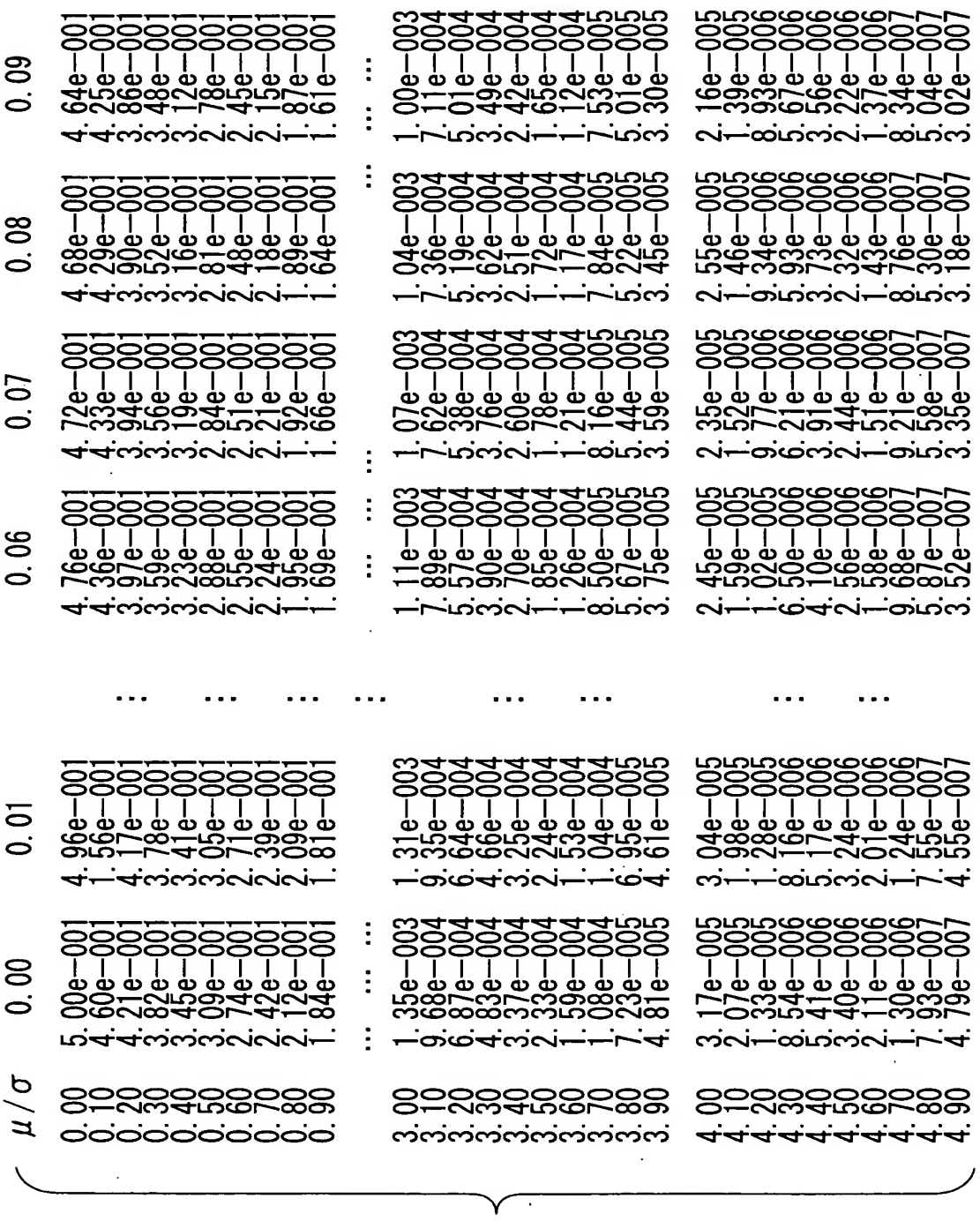

μ/σ
0.00
0.01
0.06
0.07
0.08
0.09
0.00 0.10 0.20 0.30 0.40 0.50 0.60 0.70 0.80 0.90
3.00 3.10 3.20 3.30 3.40 3.50 3.60 3.70 3.80 3.90
4.00 4.10 4.20 4.30 4.40 4.50 4.60 4.70 4.80 4.90

FIG. 26

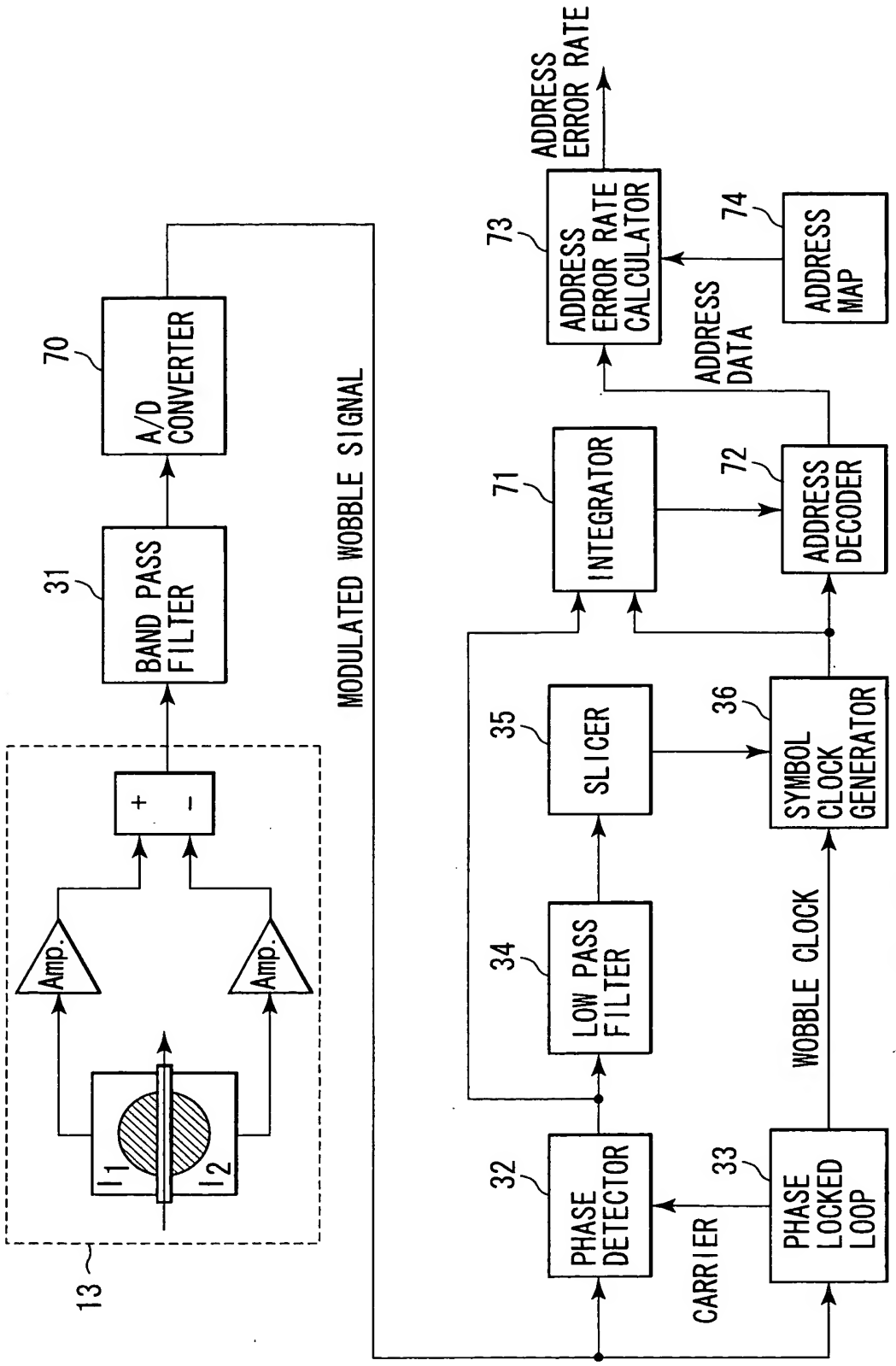

13
Amp.
Amp.
I1
I2
+
-
31
BAND PASS FILTER
70
A/D CONVERTER
MODULATED WOBBLE SIGNAL
32
PHASE DETECTOR
33
PHASE LOCKED LOOP
CARRIER
34
LOW PASS FILTER
35
SLICER
36
SYMBOL CLOCK GENERATOR
WOBBLE CLOCK
71
INTEGRATOR
72
ADDRESS DECODER
ADDRESS DATA
73
ADDRESS ERROR RATE CALCULATOR
74
ADDRESS MAP
ADDRESS ERROR RATE

FIG. 27

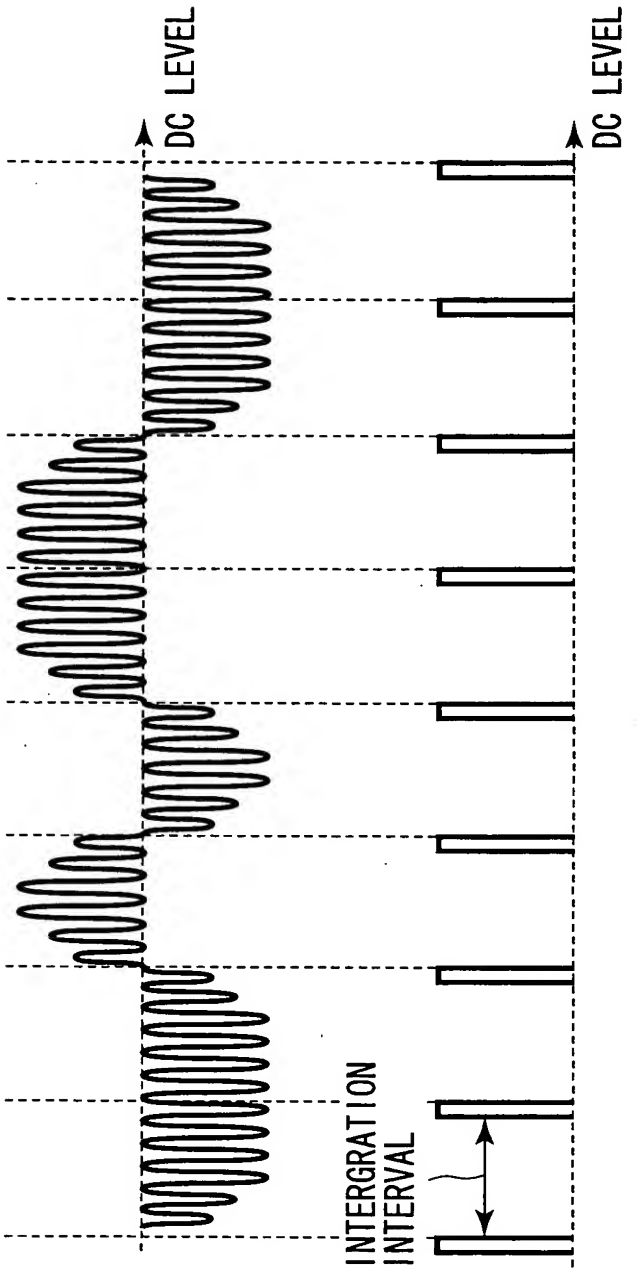


FIG. 28A

FIG. 28B

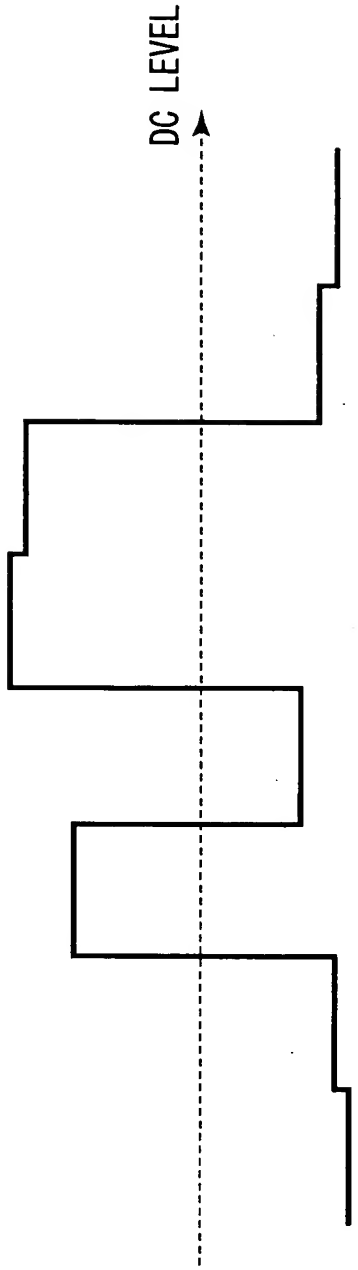


FIG. 28C

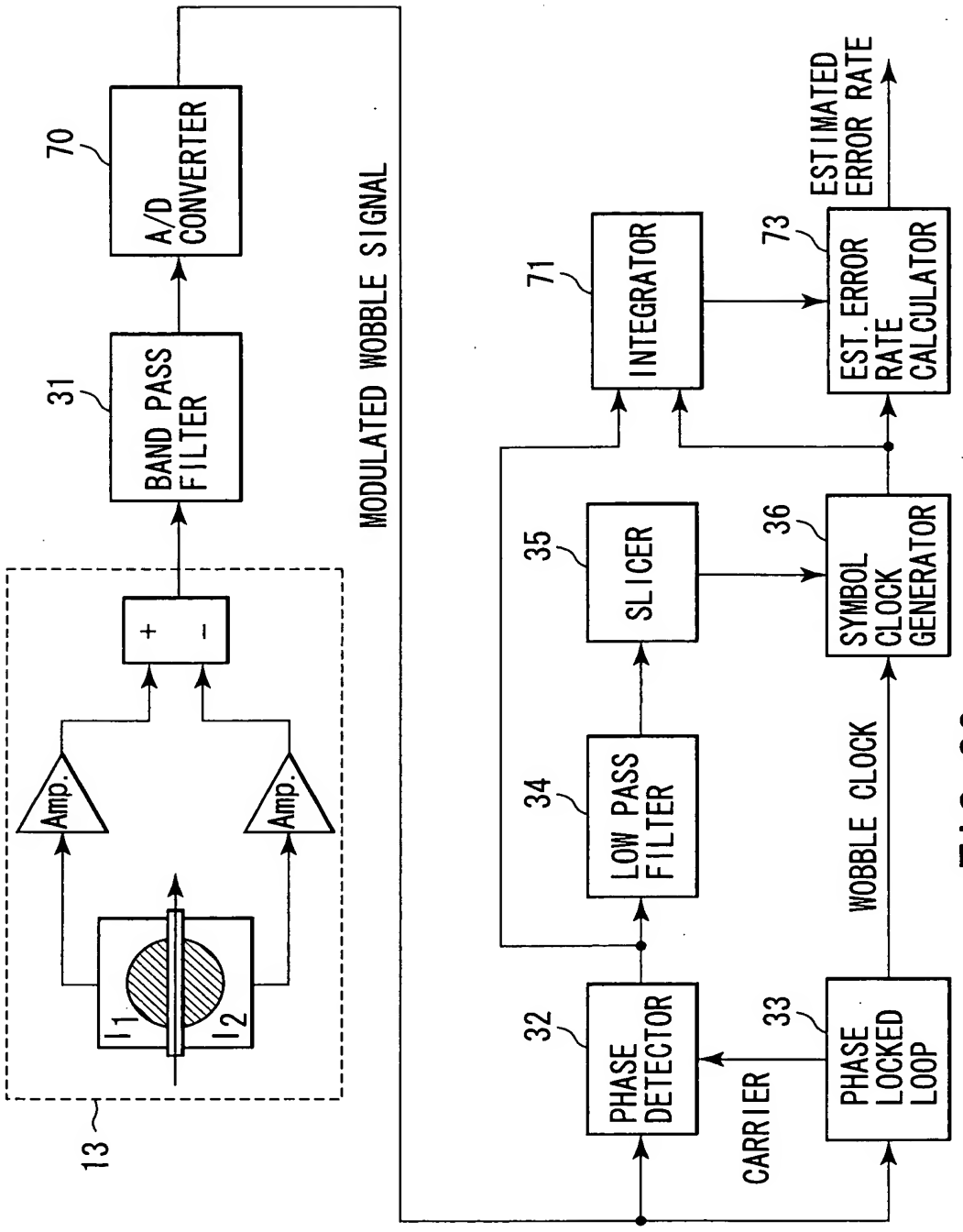

13
Amp.
Amp.
I1
I2
+
−
31
BAND PASS FILTER
70
A/D CONVERTER
MODULATED WOBBLE SIGNAL
32
PHASE DETECTOR
33
PHASE LOCKED LOOP
CARRIER
34
LOW PASS FILTER
35
SLICER
36
SYMBOL CLOCK GENERATOR
WOBBLE CLOCK
71
INTEGRATOR
73
EST. ERROR RATE CALCULATOR
ESTIMATED ERROR RATE

FIG. 29